IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A signal processing apparatus, ~~employing~~ comprising:

a second-order Volterra filter ~~for an equalizer~~ configured to equalize an input signal, wherein,

a quadratic section of said second-order Volterra filter ~~for implementing~~ configured to implement a quadratic term of said second-order Volterra filter includes a multiplication ~~means for multiplying~~ unit configured to multiply a first input signal with a second input signal to produce a product signal, [[;]]

said multiplication ~~means~~ unit including,

one or more delay ~~means~~ units connected in series with one another ~~for delaying~~ and configured to delay a signal output from said multiplication ~~means~~ unit, each by a unit time, ~~coefficient multiplying means for multiplying~~

a multiplier configured to multiply a signal output from said multiplication ~~means~~ unit and a signal output from each of said one or more delay ~~means~~ units, each with a preset coefficient, said multiplier being further configured to update each preset coefficient every unit time, and ~~summation means for summing~~

an adder configured to sum outputs of said ~~coefficient multiplying means~~ multiplier together.

2. (Currently Amended) The signal processing apparatus according to claim 1, wherein said quadratic section includes a plurality of [[said]] multiplication ~~means~~ units, one of said plurality of multiplication ~~means employing~~ units being configured to employ a signal

not delayed from said first input signal, as said second input signal, the remaining ones of said plurality of multiplication ~~means~~ units each ~~employing~~ being configured to employ a signal delayed a preset time from said first input signal, as said second input signal.

3. (Currently Amended) The signal processing apparatus according to claim 1, wherein said quadratic section includes n of said multiplication ~~means~~ units, n being an integer not less than ~~unity;~~ 1, a [[k'th]] kth one of said plurality of multiplication ~~means~~ units, k being an integer such that $1 \leq k \leq n$, ~~employing~~ being configured to employ a signal corresponding to said first input signal delayed by (k−1) times of said unit time as said second input signal.

4. (Currently Amended) A signal processing method, employing a second-order Volterra filter, for equalizing an input signal, ~~wherein~~ the signal processing method comprising:

performing a processing equivalent to a quadratic term of said second-order Volterra filter including, ~~includes a multiplication step of~~

multiplying [[said]] a first signal with [[said]] a second signal to produce a product signal; ~~a delaying step of~~

delaying [[a]] the product signal, ~~output by said multiplication step,~~ by one or more series-connected delay ~~means~~ units, each by a unit time; ~~a coefficient multiplying step of~~

multiplying [[a]] the product signal ~~output by said multiplication step~~ and a signal output from each of said ~~delaying step~~ one or more series-connected delay units, each with a preset coefficient to produce a plurality of addend signals,

updating each preset coefficient every unit time, and ~~a summing step of~~

summing the plurality of addend signals ~~plural outputs of said coefficient multiplying step~~ together.

5. (Currently Amended) A signal decoding apparatus, employing a second-order Volterra filter, ~~as an equalizer~~ for equalizing and decoding an input signal, the signal decoding apparatus comprising:

a linear section of the second-order Volterra filter, the linear section being configured to implement ~~for implementing~~ a linear term of said second-order Volterra filter and ~~for linear equalization of~~ to linearly equalize said input signal;

a quadratic section of the second-order Volterra filter, ~~for implementing~~ the quadratic section being configured to implement a quadratic term of said second-order Volterra filter and ~~for non-linear equalization of~~ to non-linearly equalize said input signal; ~~signal summing means for summing~~

a first adder configured to sum a signal output from said linear section and a signal output from said quadratic section together; and ~~most likelihood decoding means for~~

a processor configured to execute most likelihood decoding for a signal output from said ~~signal summing means;~~ first adder, the processor being further configured to detect an error, at a preset unit time, between a signal output from said first adder and a target signal, wherein

said quadratic section ~~including~~ includes a multiplication ~~means for multiplying~~ unit configured to multiply a first input signal and a second input signal together, [[;]]

said multiplication ~~means~~ unit including,

one or more series-connected delaying ~~means for delaying~~ units configured to delay signals output from said multiplication ~~means~~ unit each by [[a]] the preset unit time,

~~coefficient multiplying means for multiplying~~

a multiplier configured to multiply a signal output from said multiplication ~~means~~ unit and a signal output from each of said one or more series-connected delaying ~~means~~ units, each with a preset coefficient, said multiplier being further configured to update each preset coefficient every preset unit time based on an error detected by said processor, and ~~summing means for summing~~

a second adder configured to sum outputs of said ~~coefficient multiplying means~~ multiplier together.

6. (Currently Amended) The signal decoding apparatus according to claim 5, wherein said quadratic section includes a plurality of [[said]] multiplication ~~means~~ units, one of said plurality of multiplication ~~means employing~~ units being configured to employ a signal not delayed from said first input signal, as said second input signal, the remaining ones of said plurality of multiplication ~~means~~ units each ~~employing~~ being configured to employ a signal delayed a preset time from said first input signal, as said second input signal.

7. (Currently Amended) The signal decoding apparatus according to claim 5, wherein said quadratic section includes n of said multiplication ~~means~~ units, n being an

integer not less than ~~unity;~~ 1, a [[k'th]] kth one of said plurality of multiplication ~~means~~ units, k being an integer such that $1 \leq k \leq n$, ~~employing~~ being configured to employ a signal corresponding to said first input signal delayed by (k−1) times of said preset unit time, as said second input signal.

8. (Canceled).

9. (Currently Amended) A signal decoding method employing a second-order Volterra filter in equalizing and decoding an input signal, the signal decoding method comprising:

performing a ~~linear filtering step of implementing the~~ processing equivalent to a linear term of said second-order Volterra filter and ~~linear~~ linearly equalizing said input signal;

performing a ~~quadratic filtering step of implementing the~~ processing equivalent to a quadratic term of said second-order Volterra filter and ~~non-linear~~ non-linearly equalizing said input signal; ~~a signal summing step of~~

summing a signal output from said performing the processing equivalent to the linear ~~filtering step~~ term and a signal output from said ~~quadratic filtering step~~ performing the processing equivalent to the quadratic term together; ~~and a most likelihood decoding step of~~

most likelihood decoding a signal output from said ~~signal~~ summing ~~step~~; and

detecting an error, at a unit time, between a signal output from said summing and a target signal, wherein

said performing the processing equivalent to the quadratic ~~filtering step~~ term includes, ~~including a multiplication step of~~

multiplying [[said]] a first input signal with [[said]] a second input signal to produce a product signal; ~~a delaying step of~~

delaying [[a]] the product signal, ~~output by said multiplication step,~~ by one or more series-connected delay ~~means~~ units, each by [[a]] the unit time; ~~a coefficient multiplying step of~~

multiplying [[a]] the product signal ~~output by said multiplication step~~ and a signal output from each of said ~~delaying step~~ one or more series-connected delay units, each with a preset coefficient to produce a plurality of addend signals;

updating each preset coefficient every unit time based on the error, and ~~a summing step of~~

summing ~~outputs of said coefficient multiplying step~~ the plurality of addend signals together.

10. (New) The signal processing apparatus according to claim 1, wherein said multiplication unit further includes a shifter configured to left-shift the product signal to produce the signal output from said multiplication unit.

11. (New) The signal processing apparatus according to claim 2, wherein said multiplication unit further includes,

a first adding unit configured to add an output from a respective adder of each of the remaining ones of said plurality of multiplication units together to produce a summed signal;

a shifter configured to left-shift the summed signal to produce a shifted signal; and

a second adding unit configured to add the shifted signal and an output from the adder of the one of said plurality of multiplication units.

12. (New) The signal processing apparatus according to claim 2, wherein a step gain parameter for updating each preset coefficient of a respective multiplier of each of the remaining ones of said plurality of multiplication units is twice a step gain parameter for updating each preset coefficient of the multiplier of the one of said plurality of multiplication units.